## 17.4 A Dual-Supply 0.2-to-4GHz PLL Clock Multiplier in a 65nm Dual-Oxide CMOS Process

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PLLs are used in high-performance SoCs to generate low-jitter output clocks with wide frequency ranges. Power supply and substrate noise are the main sources of jitter in the PLL output clocks in these SoCs. On-chip voltage regulation [1] and cascoding are used to reduce the effect of power supply noise. However, as processes scale and operating voltage is reduced, less voltage headroom is available for such techniques. Typical CMOS processes have two different gate oxide layers: a thick oxide for I/O devices operating at a higher voltage, and a thin oxide for devices that operate at a lower voltage and are used for the core high-frequency digital circuits. The PLL described here uses these different devices and voltage domains to achieve low jitter and a wide frequency range. This approach has the following advantages: a) it increases the available voltage headroom, b) it reduces the VCO gain requirement to support a wide frequency range, c) it allows a better trade-off of devices for the analog and high-speed digital sections of the PLL and d) it allows the use of power supply noise rejection techniques, such as regulated supply and cascading, to improve jitter. Level-shifters are used to cross voltage domains and they are placed where their impact on jitter is minimized.

The block diagram of the charge-pump-style PLL with different voltage domains is shown in Fig. 17.4.1. The PLL architecture uses thick-oxide devices operating at 1.8V for the analog circuits and thin-oxide devices operating at 1V for high-speed sections such as the dividers. The voltage domain is crossed at the input of the phase-frequency detector (PFD). The PFD and charge-pump operate at 1.8V, which allows wider range for the loop filter voltage and reduces the VCO gain requirement. The PFD uses dual D-type flip-flop topology. The loop-filter resistor values are based on the feedback divider ratio to maintain the dynamic loop characteristics. The filter capacitor is implemented using thick-oxide NMOS devices, which have lower gate leakage.

The VCO supply is regulated using an on-chip voltage regulator to reduce the impact of power supply noise. The VCO is based on a current-starved oscillator as shown in Fig. 17.4.2. The V-to-I converter employs an active cascode circuit to provide further isolation from supply noise. The active cascode provides an optimum trade-off between headroom and output impedance [2]. The resistor R3 and capacitor C3 are used for compensation to ensure stability. The current-controlled oscillator itself uses thin-oxide devices to allow high-frequency operation. Each stage of the oscillator sees equivalent gate and wire loads. The V-to-I converter and oscillator are sized so that their maximum gate voltages do not exceed the process limit for the thin-oxide devices. The VCO output is level shifted to the 1V supply, which is used by the dividers.

The voltage regulator used to generate a quiet supply voltage for the VCO is shown in Fig. 17.4.3. A linear regulator with a PMOS transistor (M4) at the output is used to maximize the headroom available to the VCO. A bandgap reference using a vertical PNP device is used to generate the reference voltage. The regulated output voltage is compared to the bandgap reference voltage using the error correcting amplifier. The amplifier employs adaptive biasing [3], wherein the bias current is dependent on the error voltage. This biasing technique results in low quiescent current dissipation in the regulator, combined with high drive capability. The size of M4 (Fig. 17.4.3) needs to be large enough to drive current into the VCO, especially at high frequencies. This introduces a pole at the gate of M4, in addition to the dominant pole at the drain terminal, making the loop stability a concern. Furthermore, the stability is dependent on the load current in the VCO. The stability is ensured across all load current values using capacitor C1 (implemented using an NMOS device) for compensation. The worst-case simulated PSRR for the voltage regulator is better than 30dB.

The dividers are used to generate the feedback clock and various other clocks at the output of the PLL. The output clocks need to have an accurate 50% duty-cycle. Programmable dividers with a 50% duty-cycle are typically latch-based designs, which require detailed timing analysis [4,5]. This flop-based divider scheme (Fig. 17.4.4) achieves a 50% duty-cycle at high frequencies using standard CMOS logic. In order to achieve high-frequency operation and programmability, two counters are used in parallel; an odd counter and an even one. One of them counts the rising edges of the input clock and the other counts the falling edges. Each counter is incremented by 2 on every clock edge. To divide by $N$, the divide ratio is set to $N$ - 1. The rising-edge counter is reset to 0 and the falling-edge counter reset to 1. In other words, the rising-edge counter counts even numbers and the falling-edge counter counts odd numbers. The roles of these counters may be reversed depending on the input divide ratios. Once the count is reached, either by the odd or even counters, the counters are reloaded to 1 or 2 depending on which counter matched the count. One counter finishes incrementing by the time the other counter completes the comparison. Using this method, the critical path is shorter than in a conventional implementation. The toggle flop at the output guarantees the 50% duty-cycle of the output clock.

The design is implemented in a 65nm CMOS process and the measured RMS jitter (Fig. 17.4.5) in the presence of supply and substrate noise at 2GHz is 1.5ps. A wide operating range from 200MHz to 4GHz was achieved. The maximum frequency of operation of the PLL is 4GHz as shown in Fig. 17.4.6. The total power consumed from both supplies (1.8 and 1V) is 15mW. The die micrograph is shown in Fig. 17.4.7.

*Acknowledgments:*
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*References:*
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[5] P. Larsson, "High-Speed Architecture for a Programmable Frequency Divider and a Dual-Modulus Prescaler," *IEEE J. Solid-State Circuits*, pp. 744-748, May, 1996.

 

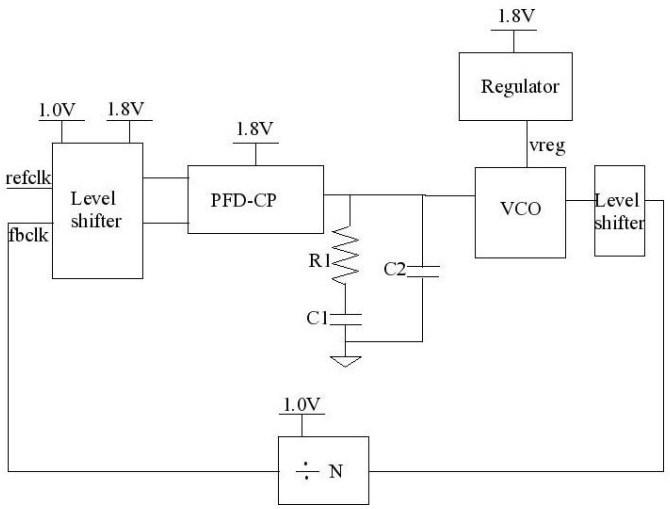


Figure 17.4.1: PLL block diagram.

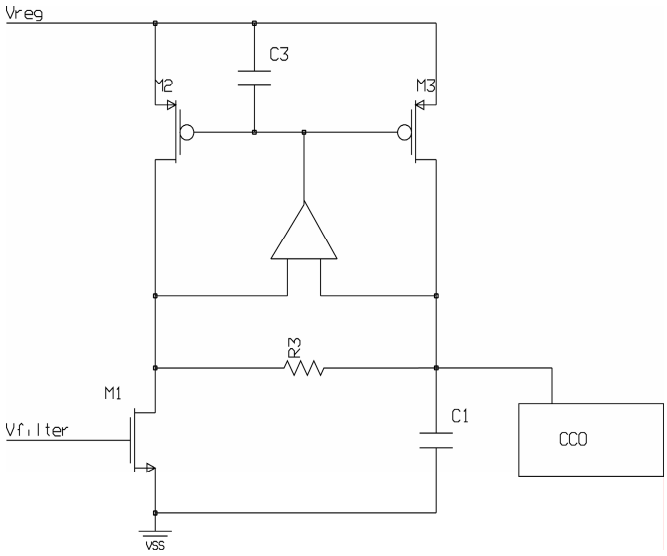


Figure 17.4.2: Voltage-controlled oscillator.

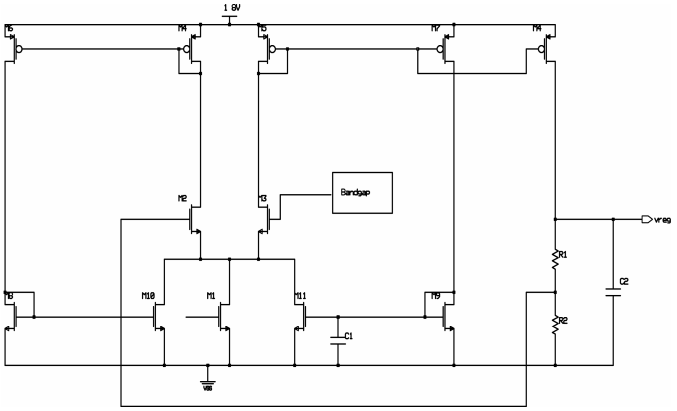


Figure 17.4.3: Voltage regulator.

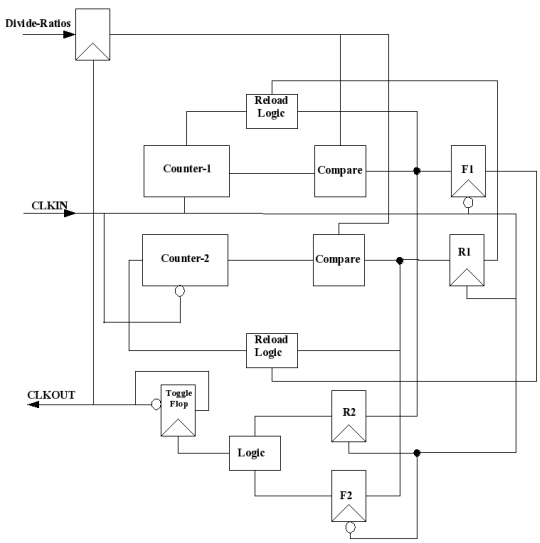


Figure 17.4.4: Programmable frequency divider with 50% duty cycle.

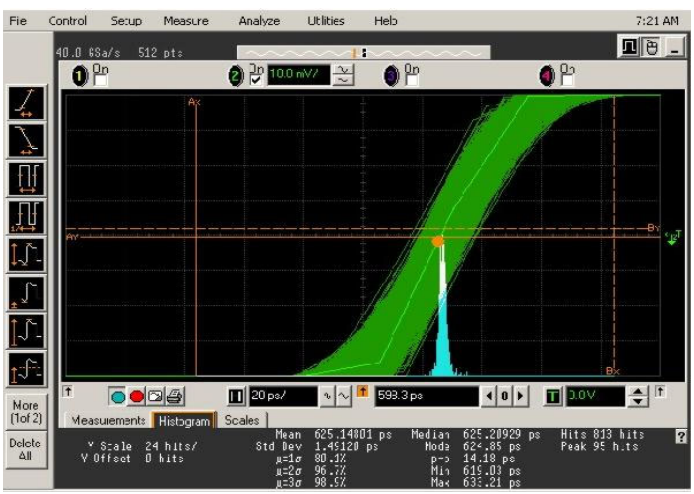


Figure 17.4.5: Measured period jitter.

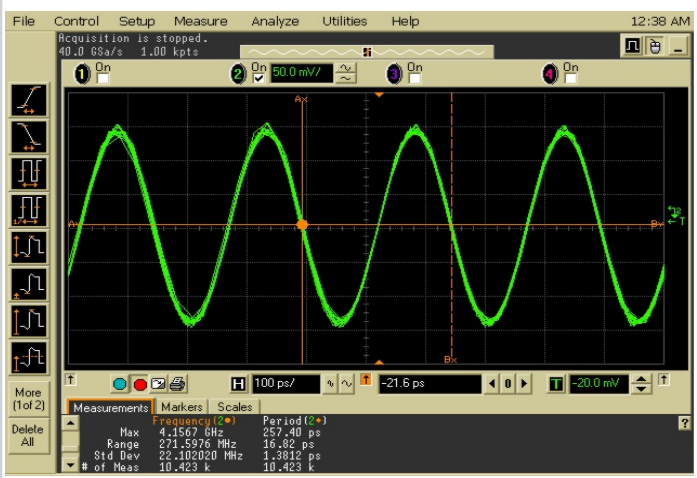


Figure 17.4.6: Measured maximum frequency of operation.

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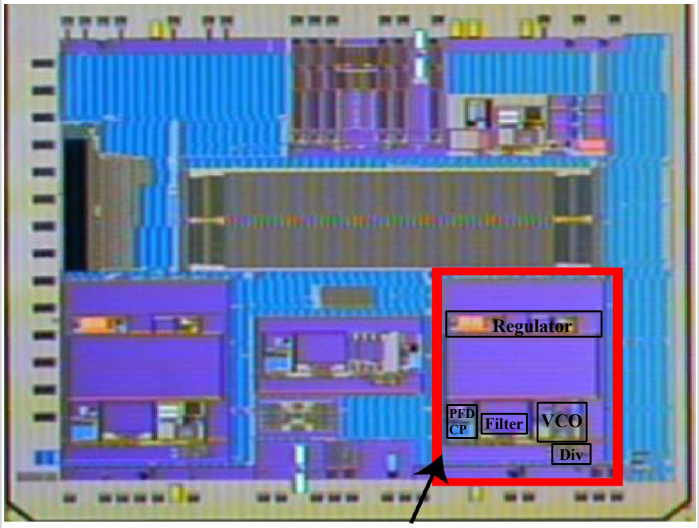


Figure 17.4.7: Die micrograph.

 